Intel® Technologies for High-Performance Computing

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Agenda

- HPC is Changing
- Server Processor Roadmap
- Performance Technologies
- Intel® Software Tools
- Summary

Intel® in the Top500*

The number of Intel based HPC systems on the Top500 list raised *from 3 to 56* over the last 3 years! Two systems now being listed in the Top10.

#5 LLNL (Lawrence Livermore National Labs) - 2304 Xeon™ processors *http://www.linuxnetworx.com/news/llnl_info.php*

#8 The National Oceanic & Atmospheric Association (NOAA) Forecast System Laboratory, 1536

#17 Louisiana State, Xeon cluster, 2207

#42 BP Houston Itanium 2 cluster, 545 (top ranked IPF cluster)

And much more…
see http://www.top500.org/

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And other recent Wins

- LANL (Los Alamos Labs) - 2050 Xeon™ processors
  http://www.linuxnetworx.com/news/lanl_info.php

UK:

- Atomic Weapons Establishment - 300 node Xeon cluster
- Southampton - 350 node Pentium® 4 & Xeon cluster
- Cambridge, Engineering Department
- Oxford University, High Engineering Physics
- Imperial College,
- etc…

HPC Inflection Point

Intel® Architecture

Can accessible, affordable technology drive off-the-chart performance?

X

Traditional HPC

Proprietary HPC

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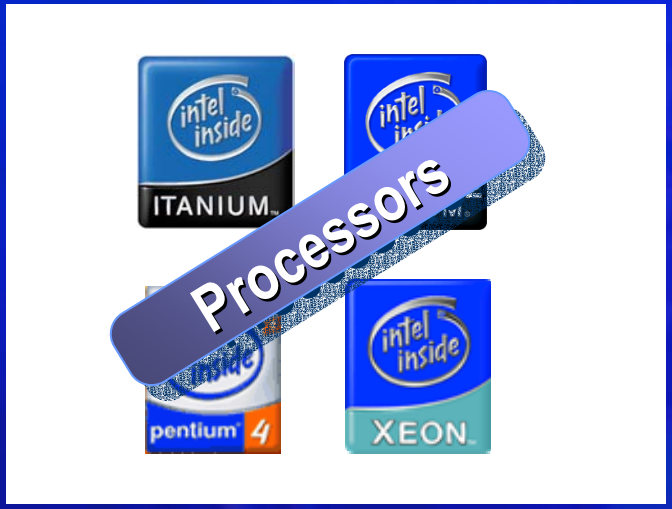
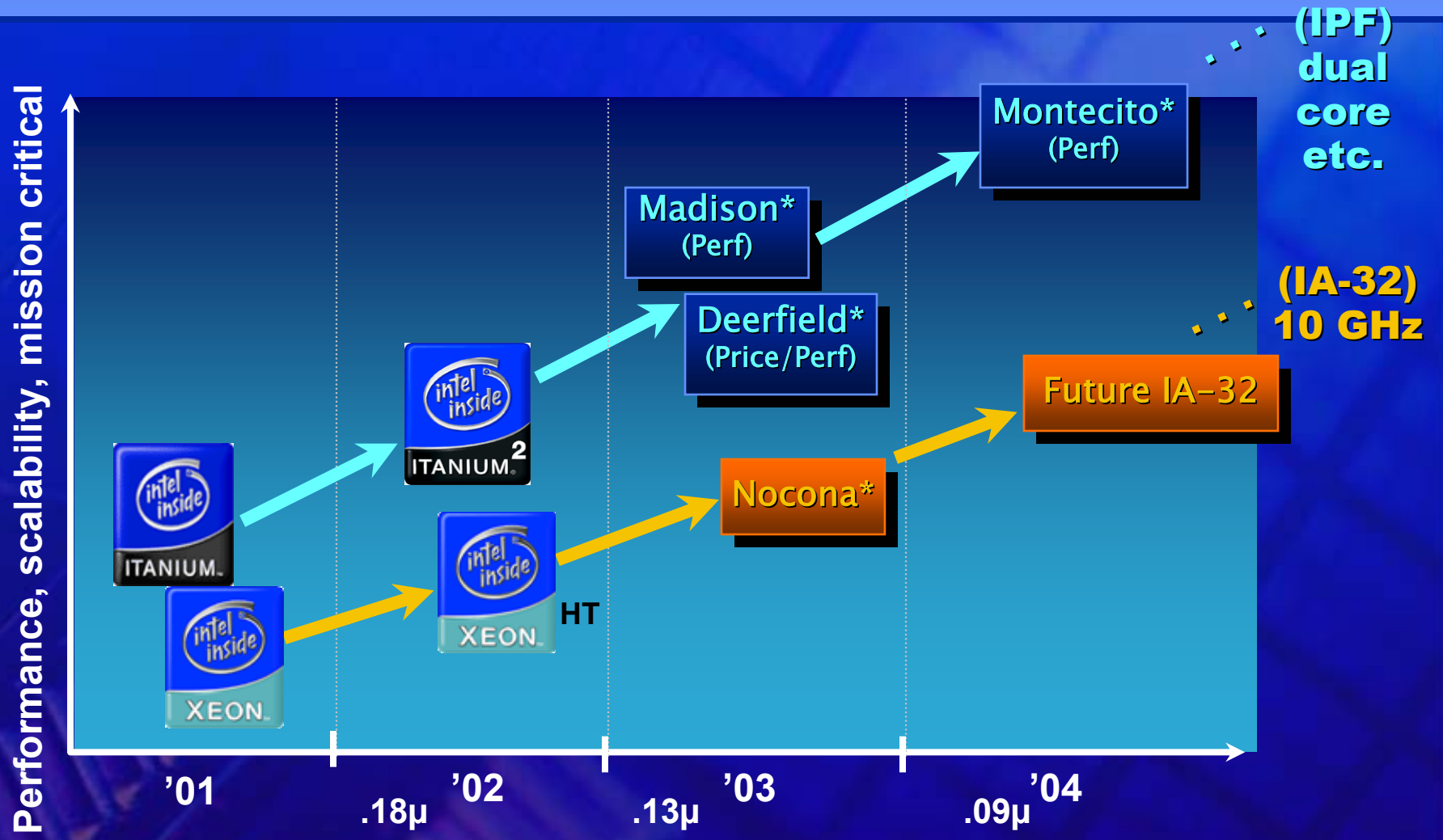
Essential Building Blocks for HPC Leadership



Server Processor Roadmap



All dates specified are target dates provided for planning purposes only and are subject to change. (*Codename)

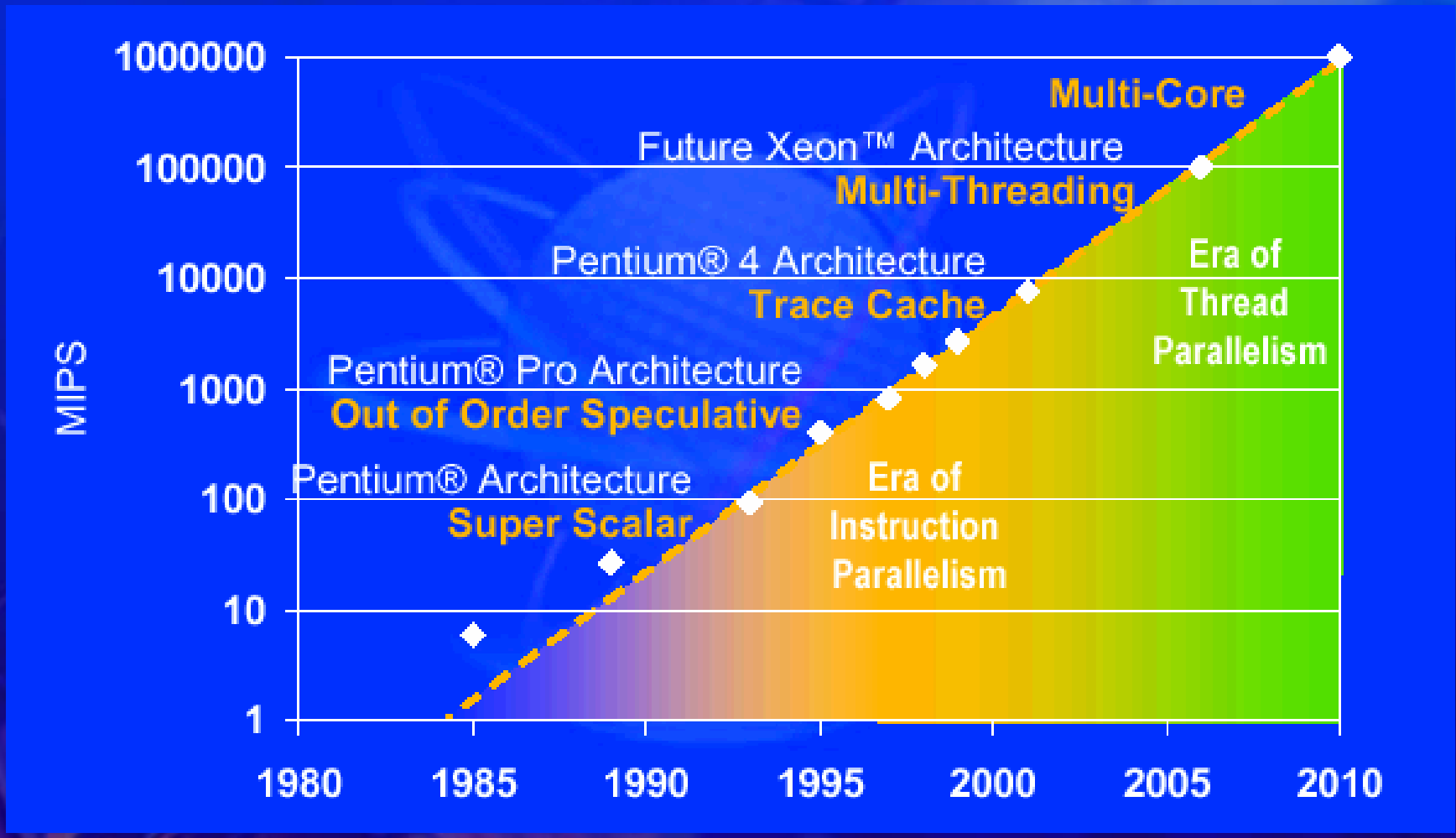
Intel® Itanium® 2 Processor and Successors Feature Comparison

	Intel Itanium 2	Madison*	Montecito*
Product Description	Second member of the Itanium Processor family	Follow-on processor to Intel Itanium 2 for performance servers/ workstations	Follow-on processor to Madison
Process	.18µ process	.13µ process	.09µ process
Frequency	900 MHz / 1 GHz	> 1 GHz	>> 1 GHz
L3 Cache	1.5 MB / 3 MB	3 – 6 MB	> 6 MB
System Bus	400 MHz (6.4 GB/s)	400 MHz (6.4 GB/s)	400 MHz (6.4 GB/s)
Transistor Count	221 Mio.	~500 Mio.	TBD

All CPUs pin-compatible with the Itanium 2 processor!

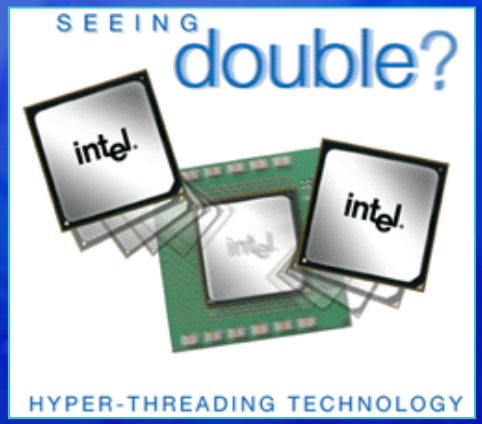
All dates specified are target dates provided for planning purposes only and are subject to change. (*Codename)

Moore's Law still on Track



Hyper-Threading™ Technology

- Executes 2 threads simultaneously
  - Of two different applications (processes)
  - Of same application (process)
- CPU maintains architecture state for 2 processors
  - 2 *logical processors* on 1 *physical processor*
  - Duplicated register set
  - Shared cache, execution units, buffers, etc.
- First implementation on Intel® Xeon™ Processors
  - Two logical processors for 5% additional die area
  - Now available in all XEON™ processors (DP & MP)
- Intel Pentium® 4 Processors followed on Nov 14th 2002 with the "Northwood Refresh" at 3.06 GHz



The world's first general-purpose simultaneous multi-threading (SMT) implementation

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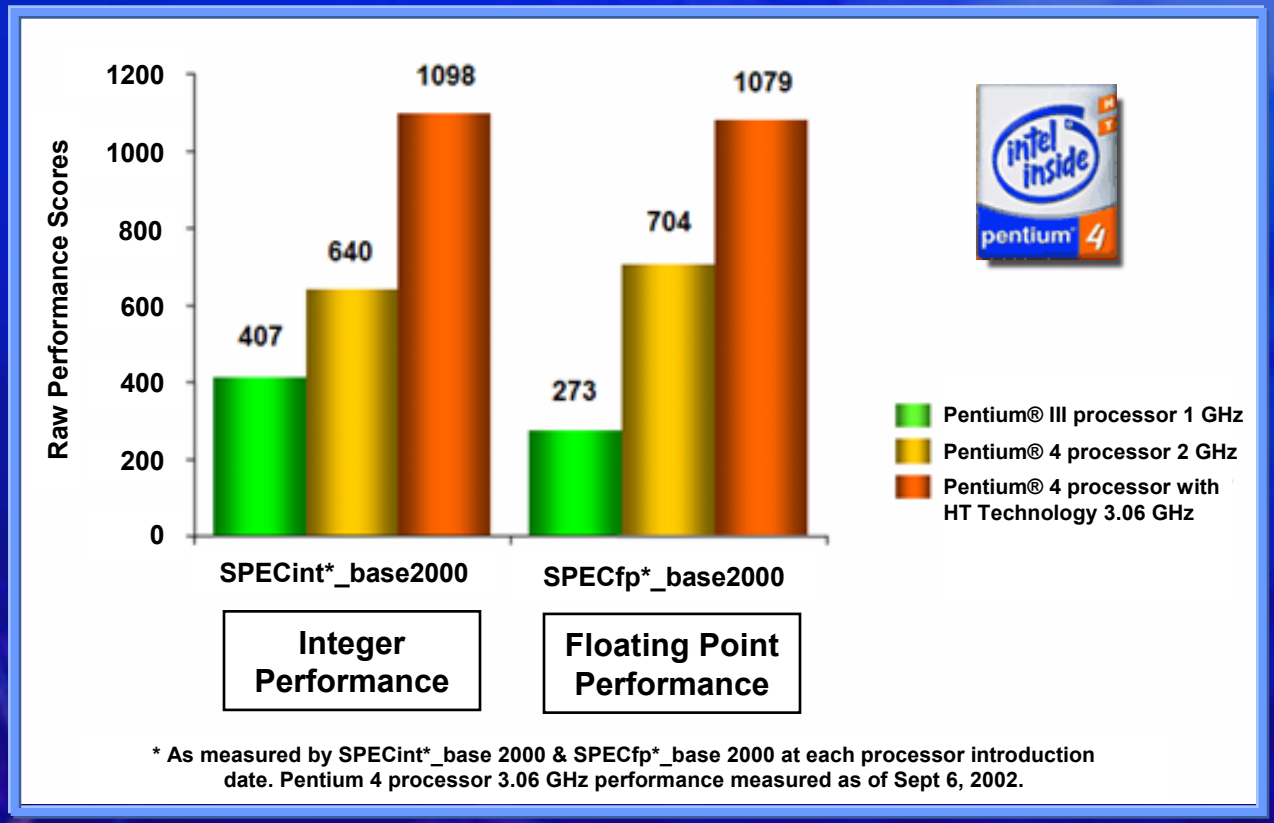
Intel® Technologies: 3.06 GHz



* As measured by SPECint*_base 2000 & SPECfp*_base 2000 at each processor introduction date. Pentium 4 processor 3.06 GHz performance measured as of Sept 6, 2002.

First processor with a SPECint_base score beyond 1000 !

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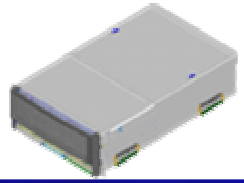
Essential Building Blocks for HPC Leadership

Itanium® 2 Systems Range

High-end Itanium® 2-based SMP systems
>2x more than Itanium !

HP 2P WS
Shipping



RackSaver DP/1U
Q4 2002

HP DP/2U
Shipping

Intel 4P/4U
Q4 2002

IBM 4P/8P/16P
Early 2003

Unisys 16P
Q4 2002

NEC 32P
Shipping

SGI 64/512P
Early 2003

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Itanium® 2 Processor
Record setting Performance

BENCHMARK	SAP (2 Tier)[1] Sales and Distribution	TPC-C[2] Transaction Processing	Linpack[3] High Performance Computing	TPC-C[4] Transaction Processing	Stream[5] Platform Bandwidth
SCALE	*4-way*	*4-way*	*32-way*	*32-way*	*64-way*
RESULT	**600 USERS**	**80.4K tpmC**	**101 GFLOPS**	**308K tpmC**	**120 GB/sec**
	WORLD RECORD	WORLD RECORD	WORLD RECORD	IA SMP RECORD	WORLD RECORD

1 Source: Itanium® 2 processor results measured on HP Server rx5670 using 4 Itanium® 2 processors 1GHz with integrated 3MB L3 cache, 24GB of memory, 528GB disk space, HP-UX 11.23, SAP rev 4.6D, Oracle 9i V.2

2 Source www.tpc.org: Itanium® 2 processor measurements done on a HP Server rx5670 using 4 Itanium® 2 processors 1GHz with integrated 3MB L3 cache, 48GB memory, HP-UX 11.23, Oracli 9iV.2, at $4.83 per tpmC

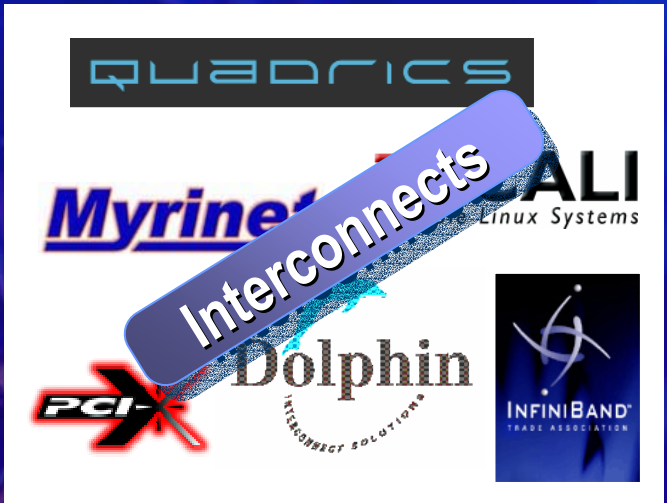
3 Source: Itanium® 2 processor measurements done on a NEC Server TX7/i9510 using 32 Itanium® 2 processors 1GHz with integrated 3MB L3 cache, 128GB memory, Linux OS.

4 Source: Itanium® 2 processor measurements done on a NEC TX7/i9510 Server using 32 Itanium® 2 processors with integrated 3MB L3 cache, 256GB memory, Windows® .NET Server 2003, Datacenter Edition, Microsoft SQL Server 2000 Enterprise Edition (64-bit) beta version, Availability date 12/31/02.

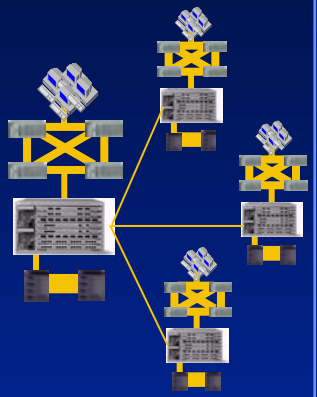
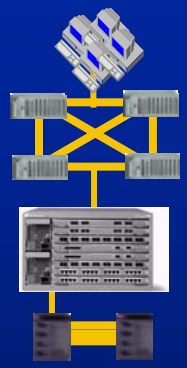
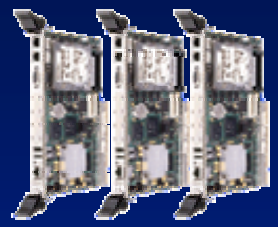
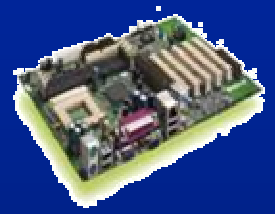
5 Source: Itanium® 2 processor measurements done on a SGI Scalable Linux System using 64 Itanium® 2 processors, 128GB memory, Linux OS.

Performance tests and ratings are measured using specific computer systems and/or components and reflect the approximate performance of Intel products as measured by those tests. Any difference in system hardware or software design or configuration may affect actual performance. Buyers should consult other sources of information to evaluate the performance of systems or components they are considering purchasing. For more information on performance tests and on the performance of Intel products, reference www.intel.com/procs/perf/limits.htm or call (U.S.) 1-800-628-8686 or 1-916-356-3104

Essential Building Blocks for HPC Leadership



Future Interconnect & Storage

Inter-Facility	Inter-System	Intra-System	Intra-Board
			
Site to Site Data Center to Data Center	Rack to Rack	Blade to Blade Within the Rack Line Cards	Chip to Chip Add-in Card

Ethernet/iSCSI

InfiniBand™/FC

PCI Express/S-ATA

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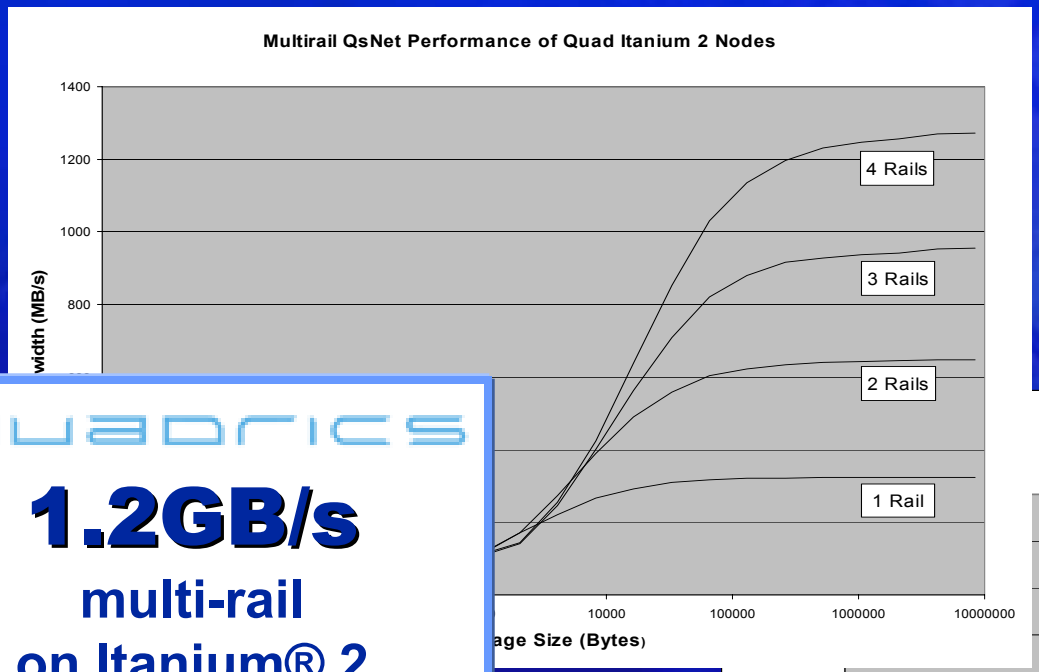
Interconnect Performance



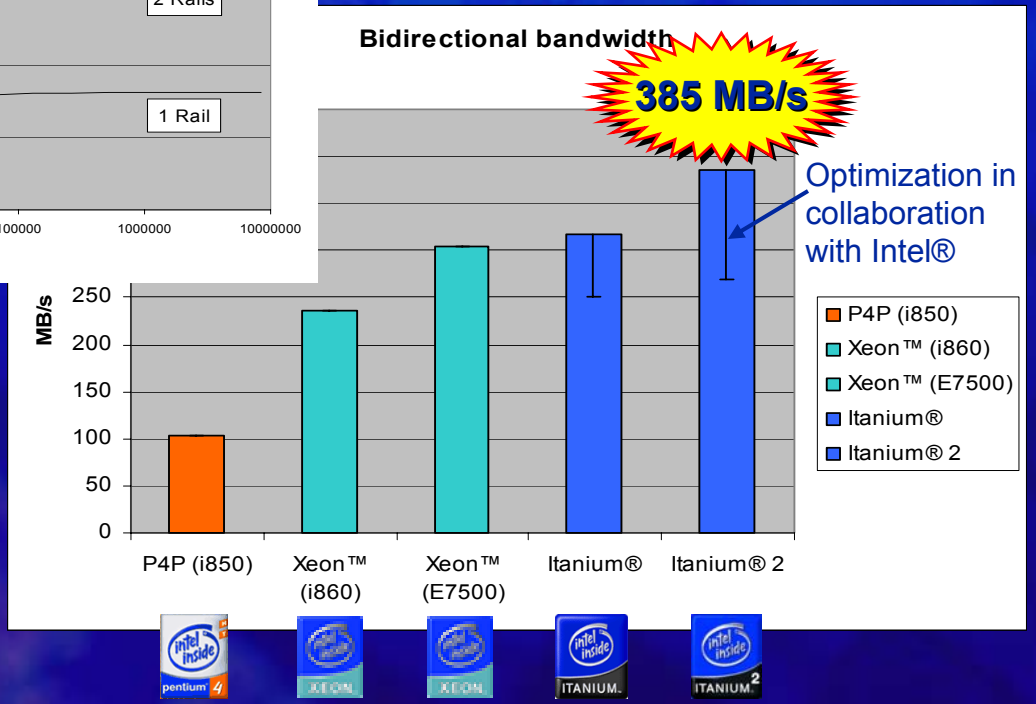
QUADRICS

1.2GB/s

multi-rail

on Itanium® 2

SCALI
Scalable Linux Systems



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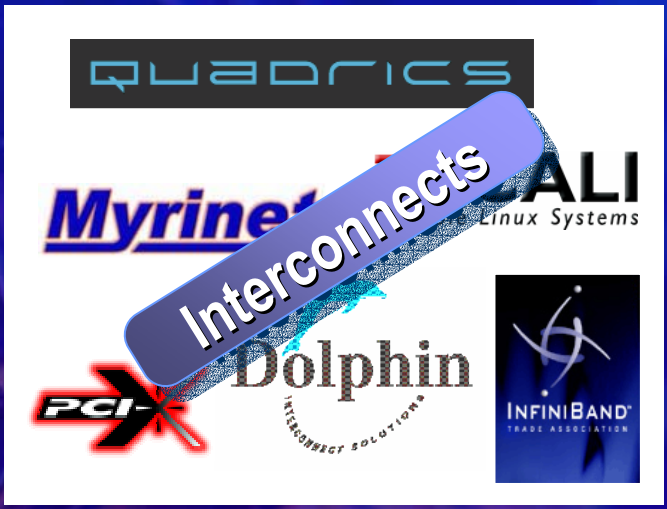
Essential Building Blocks for HPC Leadership

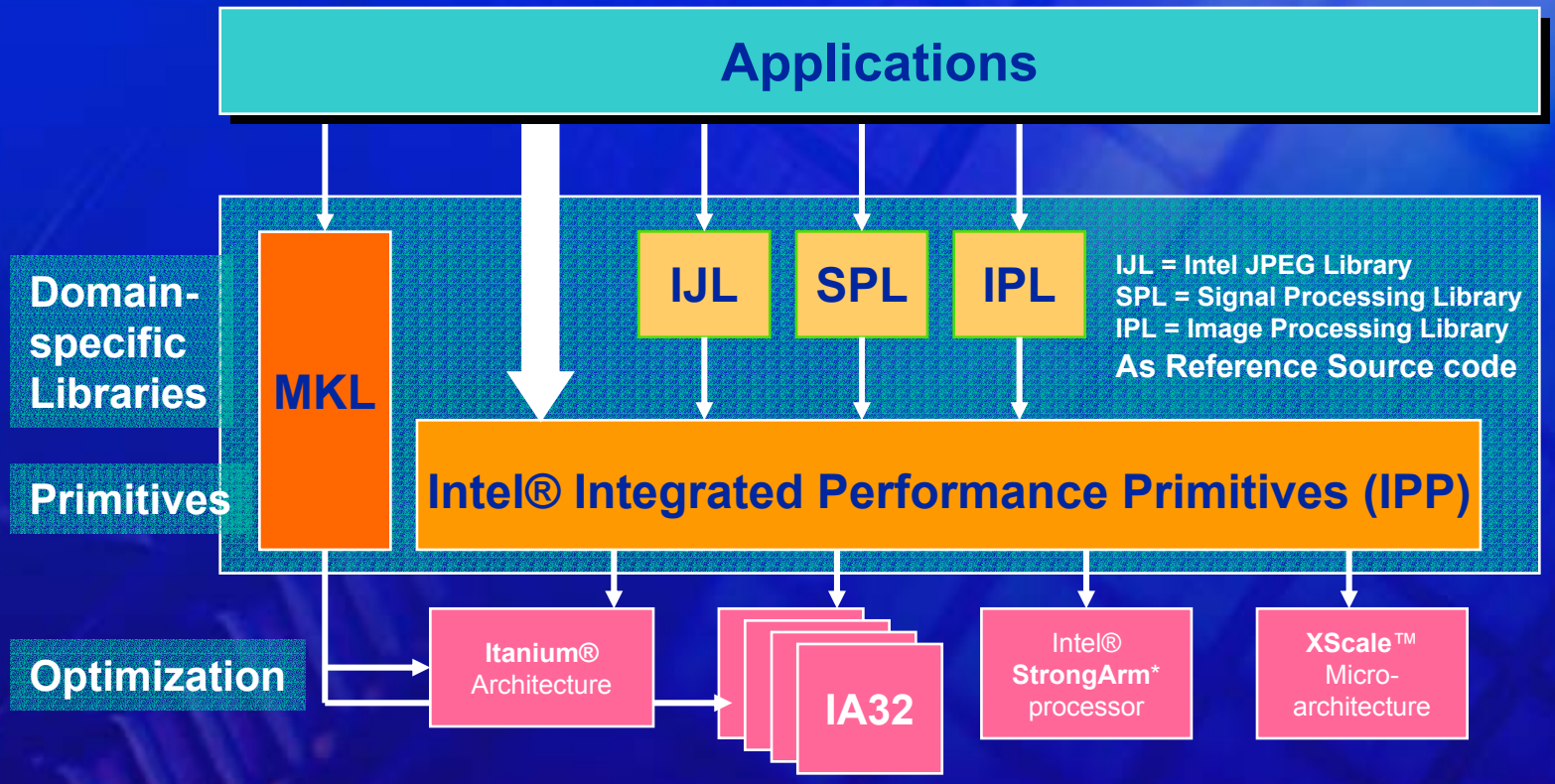


Intel® Compilers

- Ver. 7.0 publicly released on Nov 21
- Targeting Windows* and Linux*, IA-32 and IA-64
- Optimized for the latest Intel microprocessors including
  - Intel® Itanium® 2 Processor
  - Intel® Xeon™ Processor
- Intel 7.0 Fortran Compiler acting as a bridge to Intel Visual Fortran 8.0
  - Many CVF command line spellings and features accepted
  - Plus e.g. REAL*16, COMPLEX*32 and dynamic COMMON support, etc.

http://developer.intel.com/software/products/compilers/

Intel® Performance Libraries



Expanded functionality & full platform integration

Intel® Math Kernel Library

- MKL 5.2 SP1
  - BLAS (Basic Linear Algebra Subroutines; CBLAS)
  - Large subset of LAPACK
  - FFTs (Fast Fourier Transforms)
  - VML (Vectorized transcendental functions)
  - Extensive PDF manual
- MKL 6.0 beta
  - http://www.intel.com/software/products/mkl/mkl60
  - New set of discreet Fourier transforms (DFTs)
  - New set of vector statistical functions (VSL)
  - Includes some important optimizations (e.g. ITP2)
  - Public release targeted for early ’03
- Future plans for cluster SW: initially ScaLAPACK, DFTs later; eventually a direct sparse solver

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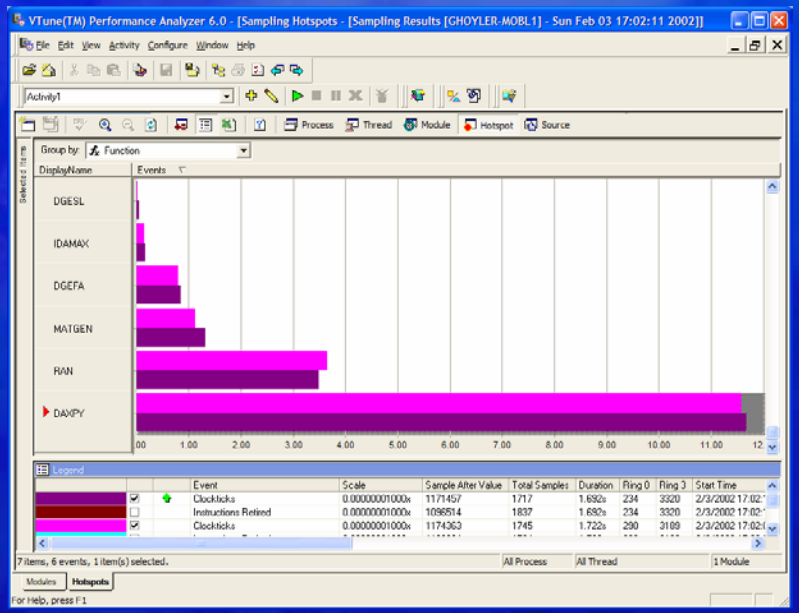
VTune™ Performance Analyzer 6.1

- Identifies performance bottlenecks in source code with low intrusion event and time based technology
  - Interrupt-based sampling using CPU performance counters
- Features:
  - Supports Intel® Pentium® 4, Xeon™ and Itanium® processors
  - Linux* remote data collectors (32- and 64-bit)
  - HT, .Net* and C# support added
  - Also supports C/C++, Fortran, Java* SDK 1.3 & 1.4, Assembler, Visual Basic*



"Hot spot" profile

Native Linux* version currently in beta

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Intel® SW Tools Resellers

- **UK Resellers**
  - Polyhedron, Greymatter, (U.K.)

Over 1200 Additional Tools Distributors, VARs and Resellers since January 2002

- **Recent New Value Added Reseller Agreements**

Summary

- The Industry's Leading Architecture is redefining Servers and HPC: HPC clearly trends towards commodity systems around Intel® Architecture
- Intel is delivering innovative performance technologies allowing to stay on track with Moore's Law for the next decade
- Intel software tools help to get the most out of the Intel Architecture:
  - Intel Compilers (C/C++ and FTN)
  - Intel Libraries (MKL, IPP)
  - VTune™ Performance Analyzer & Threading Tools

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Thank You !

intel.com/go/hpc

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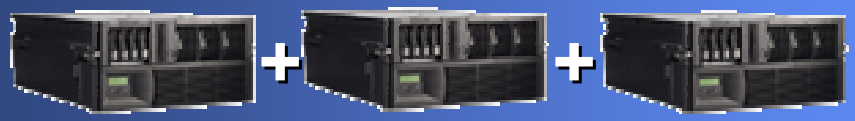
Scaling "Right"
Intel® Based Servers Scale Right

Scale Up

Scale Up on 8-way and above servers

Scale Up on 4 and 8-way servers, then **Scale Out** on HPC clusters

Scale Out with HPC clusters on 1 to 2-way servers



Scale Out

7.0 Compiler Overall Improvements

- Itanium® 2 Code Generation
  - First compiler generating Itanium 2 specific code (same instr. set as for Itanium but different instr. mix)
  - New options -tpp1/-tpp2 for Itanium rsp. Itanium-2 (default is Itanium® 2 scheduling)
- Better OpenMP* 2.0 support (but not all features)
- Much improved automatic parallelization
- Enhanced loop optimizations
- Improved binary compatibility with GCC
- Can build Linux* kernel (after some minor modifications)
- More and better reporting
- Many “internal” switches now documented
- Training Tutorial:

  “Enhancing Performance with the Intel® Compiler“

Intel® Performance Primitives

- A library of numeric, signal, image, graphic and multimedia processing functions, highly-optimized, processor-specific code
- Current Version 2.0 includes:
  - Linux* 64 bit support
  - Small matrix operations and Vector math support benefiting small-scale numeric application programming requirements
  - Audio coding and video primitives for MP3 decode, JPEG, MPEG-4 decode, and H.263 decode.
- Version 3.0 coming soon

http://developer.intel.com/software/products/perflib/